REMARKS

The present Amendment is presented in response to the Office Action. Claims 1, 9, 10, 19, 25, and 26 are amended. Claims 1-26 remain pending.

Reconsideration of the application is respectfully requested in view of the above amendments to the claims and the following remarks. For the Examiner's convenience and reference, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

I. GENERAL CONSIDERATIONS

A. Claim Amendments and/or Cancellations

With particular reference to the claim amendments, Applicant notes that while claims 1, 9, 10, 19, 25, and 26 have been amended herein, such amendments have been made in the interest of expediting the allowance of this case. Notwithstanding, Applicant, may, on further consideration, determine that claims of broader scope than those now presented are supported. Accordingly, Applicant hereby reserves the right to file one or more continuing applications with claims broader in scope than the claims now presented.

Consistent with the points set forth above, Applicant submits that neither the claim amendments set forth herein, nor any other claim amendments, claim cancellations or statements advanced by the Applicant in this or any related case, constitute or should be construed as, an implicit or explicit surrender or disclaimer of claim scope with respect to the cited, or any other, references.

B. Remarks

Applicant respectfully notes that the remarks herein do not constitute, nor are they intended to be, an exhaustive enumeration of the patentable distinctions between any cited references and the invention, example embodiments of which are set forth in the claims of this application. Rather, and in consideration of the fact that various factors make it impractical to enumerate all the patentable distinctions between the invention and the cited art, as well as the fact that the Applicant has broad discretion in terms of the identification and consideration of the base(s) upon which the claims distinguish over the cited references, the distinctions identified and discussed herein are presented solely by way of example. Consistent with the foregoing, the

discussion herein is not intended, and should not be construed, to prejudice or foreclose contemporaneous or future consideration by the Applicant, in this case or any other, of: additional or alternative distinctions between the invention and the cited references; and/or, the merits of additional or alternative arguments.

Applicants note as well that the remarks, or a lack of remarks, set forth herein are not intended to constitute, and should not be construed as, an acquiescence, on the part of the Applicants: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case. Applicants reserve the right to challenge the purported teachings and purported prior art status of the cited references at any appropriate time.

II. CLAIM REJECTIONS UNDER 35 U.S.C. §102(e)

The Examiner rejected claim 14 under 35 U.S.C. § 102(e) as being anticipated by United States Patent Publication No. 2004/0179138 to *Wang et al.* ("*Wang*"). Applicants respectfully traverse the rejection.

Claim 14 recites, among other things:

> receiving an asserted synchronization signal from a phase locked loop…
>
> determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency; and
>
> asserting a lock signal if the phase locked loop has locked onto a data signal."

However, Applicants respectfully submit that the Examiner has not established that *Wang* teaches the aforementioned limitations.

The Examiner repeated the same rejection almost verbatim as it appeared in the previous Office Action. *See Office Action*, p. 9. As noted in Applicants' previous response, however, **the rejection completely fails to specify what element(s) of *Wang* purportedly correspond to the claimed "synchronization signal."** The response to arguments section of the Office Action similarly fails to **clarify what, if any, portion(s) of *Wang* are believed by the Examiner to correspond to the claimed "synchronization signal."**

As one possibility, it might be the case that the Examiner is implying that a signal is inherently output by PLL 3 and received by phase-locked loop (PLL) detection circuit 17, which in turn produces an unlocked or locked signal. *See Office Action*, p. 3 ("The status of the phase locked loop must be determined in order to output a signal indicating an unlocked or locked signal.") However, the Examiner has not established that *Wang* teaches the particular nature of any signals that might be passed between PLL 3 and PLL detection circuit 17, much less whether any such signal is a "synchronization signal," as claimed. Moreover, the Examiner has not pointed to any teaching in *Wang* that the Examiner believes to correspond with the specific claim limitation of "determining whether [a PLL 3 output signal] is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency."

Therefore, should the Examiner continue to allege that *Wang* teaches a "synchronization signal," as claimed, **clarification is respectfully requested as to where *Wang* purportedly discloses a "synchronization signal"** and **where *Wang* allegedly discloses determining whether the signal is "caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency**," as claimed.

Since the Examiner has failed to establish that *Wang* discloses each and every element of claim 14, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn.

III. CLAIM REJECTIONS UNDER 35 U.S.C. § 103

A. Summary of Rejections and Obviousness Standard

The Examiner rejected claims 1-3, 9, 10, and 15 under 35 U.S.C. § 103 as being unpatentable over *Wang* in view of "The 555 Timer Tutorial" by Tony van Roon ("*van Roon*"); rejected claims 4 and 5 under 35 U.S.C. § 103 as being unpatentable over *Wang* in view of *van Roon* as applied to claim 3 above and further in view of "Transistors" at www.electronics-tutorials.com ("*Transistors Tutorial*"); rejected claims 16 and 17 as being unpatentable over *Wang* as applied to claim 14, and further in view of U.S. Patent No. 5,886,748 to *Lee* ("*Lee*"); rejected claims 6, 7, 11, and 12 as being unpatentable over *Wang* and *van Roon* as applied to

claim 2, and further in view of *Lee*; rejected claim 8 as being unpatentable over *Wang*, *van Roon*, and *Lee*, as applied to claim 7, and further in view of "Phase-Locked Loop Protocol Scheme for a Synchronization Field," IBM Technical Disclosure Bulletin, May 1990 ("*IBM TDB*"); rejected claim 13 as being unpatentable over *Wang*, *van Roon*, and *Lee*, as applied to claim 12, and further in view of *IBM TDB*; and rejected claim 18 as being unpatentable over *Wang* as applied to claim 14, and further in view of *IBM TDB*.

As in discussed in the following remarks, Applicants traverse the Examiner's rejections for obviousness on the grounds that the Examiner has not shown that the references—either individually or in combination—teach or suggest each and every element of the rejected claims.

Applicants respectfully note at the outset that in order to establish a *prima facie* case of obviousness, it is the burden of the Examiner to demonstrate that the prior art reference (or references when combined) teaches or suggests all the claim limitations. *See MPEP* § 2143. Moreover, "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." *See MPEP* § 2141.III; *KSR Int'l Co. v. Teleflex, Inc.*, 82 USPQ2d 1385 (U.S. 2007). Furthermore, "[i]f [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *See MPEP* § 2143.01.V.

B. Rejections Based on Wang

1. Claims 1-8

Amended claim 1 recites, among other things, "...a phase locked loop adapted to...keep [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal; and a timing circuit adapted to measure a period of time that the synchronization signal is asserted and to produce a lock signal if the synchronization signal is asserted for at least a specified period of time."

The Examiner asserted that *Wang* discloses a circuit that produces a lock signal if a synchronization signal is asserted for at least a pause time, Tp. *See Office Action*, p. 10. However, as with claim 14 discussed above, it is unclear from the Examiner's remarks **what portion of *Wang* is believed by the Examiner to correspond to the claimed "synchronization signal**." Thus, **clarification on this point is respectfully requested**.

In the interests of advancing prosecution, and though Applicants are unclear on this point, it may be the view of the Examiner that the locked/unlocked status of PLL 3 in *Wang* corresponds to the claimed "synchronization signal." *See Office Action*, p. 5 ("[*Wang*] indicates that the phase locked loop connected to the coincidence detection circuit 7 is paused so the locked/unlocked status of the PLL can be examined for a time period of Tp.") (citing *Wang*, paragraphs [0031] and [0043]).

However, the Examiner has failed to assert how a locked/unlock status of a circuit is purported to correspond to a signal, much less to a "synchronization signal" that a phase locked loop is adapted to "keep…asserted as long as the phase locked loop is locked onto a data signal," as claimed. In fact, if the locked/unlocked status of the PLL 3 is not implemented as a signal, there would seem to be little purpose for PLL detection circuit 17, which "determines whether the PIF PLL 3 is in a locked state" and accordingly outputs a "1" or a "0" signal. *See Wang*, paragraph [0033]. Conversely, if the Examiner believes the locked/unlocked status of PLL 3 corresponds to the claimed "lock signal," it is unclear what element(s) of *Wang* might be alleged to correspond to the claimed "synchronization signal."

Moreover, as the name "pause time" implies (*see Wang*, paragraph [0051]), time Tp is merely used to pause an activity, to allow "coincidence detection circuit 7 to detect whether synchronization of the horizontal oscillator 8 with the incoming RF signal has been achieved…." *See Wang*, paragraph [0043]. As presently understood then, the pause time, Tp, is not used as a "specified period of time" to be measured against "a period of time that the synchronization signal is asserted," as required by claim 1.

Therefore, the Examiner has failed to establish that *Wang* teaches or suggests each and every element of claim 1. Furthermore, the Examiner has not established that any of *van Roon*, *Transistors Tutorial*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, cures the deficiencies of *Wang*. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for obviousness and respectfully submit that the rejection of claim 1, and corresponding dependent claims 2-8, should be withdrawn.

2. Claims 9-13

Claim 9 recites, among other things, "a controller chip having a phase locked loop that … is adapted to operate in a locked mode that asserts the synchronization signal so long as the

phase locked loop is locked onto a data signal; and a translation circuit that converts the synchronization signal from the controller chip to a lock signal...." In contrast, the Examiner has not established that *Wang* discloses the aforementioned limitations. For example, the Examiner has not pointed to any description in *Wang* that the Examiner believes to correspond to the claimed "translation circuit."

In the Examiner's response to arguments, various different circuits/components of *Wang* are discussed, including detector circuit 7, control circuit 19, and horizontal oscillator 8. However, the Examiner has not specified which of these, if any, is believed to correspond to the claimed "translation circuit," thus leaving Applicants to guess at what the Examiner believes to be the correspondence between *Wang* and the elements of claim 9. This much, however, Applicants respectfully decline to do, inasmuch as the burden to establish *prima facie* obviousness is the burden of the Examiner. Accordingly, should the Examiner continue to maintain the same ground of rejection against claim 9, Applicants respectfully request, in the interests of compact prosecution, that the Office **identify, with specificity sufficient to support a *prima facie* case of obviousness, which element(s) of *Wang* the Examiner believes to correspond to the claimed "translation circuit."**

Applicant notes further that the Examiner has not shown that *Van Roon*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, cures the deficiencies of *Wang*. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for obviousness and respectfully submit that the rejection of claim 9, and corresponding dependent claims 10-13, should be withdrawn.

3. Claims 15-18

Applicants respectfully submit that insofar as the rejections of claims 15-18 rely on the unsupported assertions regarding the disclosure of *Wang* advanced by the Examiner in connection with the rejection of claim 14, such rejection lacks an adequate foundation, for at least the reasons outlined at section II above. Furthermore, the Examiner has not shown that *van Roon*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, cures the deficiencies of *Wang*. Accordingly, the rejections of claims 15-18 should be withdrawn.

C. Rejections Based on Hirai

The Examiner rejected claims 19 and 20 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,794,944 to *Hirai* ("*Hirai*") in view of *van Roon*; rejected claim 21 as being unpatentable over *Hirai* and *van Roon*, as applied to claim 20, and further in view of *Transistors Tutorial*; and rejected claims 22-26 as being unpatentable over *Hirai* and *van Roon*, as applied to claim 19, and further in view of *IBM TDB*.

Applicants traverse the Examiner's rejections for obviousness on the grounds that a person of ordinary skill in the art would have no reason to combine the prior art elements in the manner claimed because the proposed combination would render *Hirai* unsatisfactory for its intended purpose.

Claim 19 requires, among other things, "a comparator circuit adapted to compare the output signal [from a timing circuit] with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time."

The Examiner proposed combining a comparison circuit 23 in *Hirai* with a timing circuit in *van Roon*. *See Office Action*, p. 18. However, comparison circuit 23 compares count values of counters 21 and 22 (*see Hirai*, Abstract), whereas the timing circuit of *van Roon* outputs a timing pulse having a predetermined duration time (*see van Roon*, p. 7). As presently understood then, the combination proposed by the Examiner would result in a configuration where the comparison circuit 23 of *Hirai* would compare a count value from one of counters 21 and 22 with the timing pulse from the *van Roon* timing circuit. However, it is not apparent that a count value (*Hirai*) is the same as a timing pulse (*van Roon*), nor has the Examiner established as much. Thus, the comparison performed by the modified circuit 23 of *Hirai* would not be feasible and/or would at best yield meaningless results and the device would be unsatisfactory for its intended purpose of optimizing a lock detection time. *See Hirai*, Abstract.

Furthermore, the Examiner has not shown that *Transistors Tutorial* and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of the proposed combination of *Hirai* and *van Roon*. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness and respectfully request that the rejection of claim 19, and corresponding dependent claims 20-26, be withdrawn.

CONCLUSION

In view of the remarks submitted herein, Applicant respectfully submits that each of the pending claims 1-26 is in condition for allowance. Therefore, reconsideration of the rejections is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that could be clarified in a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 28th day of February 2008.

Respectfully submitted,

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